REMARKS

Claims 1-8 are pending in the present application.

I. FORMAL MATTERS

A. Claim to Priority

Applicant notes with appreciation the Examiner's acknowledgement of the claim to foreign priority under 35 U.S.C. § 119(a)-(d) or (f) and indication that the certified copies of the priority documents have been received.

B. Drawings

Applicant notes with appreciation the Examiner's withdrawal of the objection to Figs. 5, 6 and 7 in light of the argument presented in the Amendment filed on August 18, 2005.

C. Rejection of Claim 8 Under 35 U.S.C. 112, First and Second Paragraphs

Applicant notes with appreciation the Examiner's withdrawal of the rejection of claim 8 under 35 U.S.C. § 112, first and second paragraphs, in light of the Amendment filed on August 18, 2005.

II. PRIOR ART REJECTION

Claims 1-8 are rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 6,211,849 (Sasaki). This rejection is traversed.

As provided in MPEP § 2131: "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). That is: "[t]he identical invention must be shown in as complete detail as is contained in the ... claims". *Richardson v Suzuki Motor* Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir 1989).

In deciding the issue of anticipation, the trier of fact must identify the elements of the claims, determine their meaning in light of the specification and prosecution history, and identify corresponding elements disclosed in the allegedly anticipating reference (emphasis added, citations in support omitted).

Claim 1

Regarding the anticipation rejection on claim 1, Applicant respectfully submits that the Examiner has not demonstrated that Sasaki teaches or suggests every feature recited in claim 1. Therefore, Applicant submits that the Examiner has not formed a prima facie case of anticipation.

Firstly, Applicant submits that Sasaki does not teach or suggest the "timing control section" as recited in claim 1. The Examiner asserts that the "timing control section" is disclosed by the "control logic section" in Sasaki. However, Applicant submits that Sasaki discloses a control logic CT "for sequentially supplying the pixel data signal output from the first latch circuit 5 to the predetermined number of signal lines ..." and not to any subsequent driver IC 1 (emphasis added) (see column 4, lines 59-63 and Figure 4). In contrast, claim 1 requires "a timing control section for generating a timing control signal for controlling at least one of the row electrode driving circuit and the column electrode driving circuit".

This argument is further reinforced by column 5, lines 5-12 wherein Sasaki discloses that signals supplied via the input pad portion 2 into a driver IC 1 are distributed into two transmission paths. One of the transmission paths is used to supply these signals to the control logic CT, and the other is used to shape the waveforms of these signals and output the shaped signals to the next driver IC 1 via its output pad portion 3.

Therefore, Sasaki clearly discloses two separate transmission paths and the signals following the transmission path to the control logic CT are not output to the next driver IC 1 via the output pad portion 3. Furthermore, Figure 4 also clearly shows no logical signal flow connection permitting signals to flow from control logic CT to output pad portion 3. Hence, it appears impossible for the control logic CT to generate a timing control signal for controlling any subsequent driver IC 1.

Accordingly, for at least the reasons as discussed in details above, Sasaki fails to disclose the timing control section as recited in claim 1.

Secondly, Applicant submits that Sasaki does not teach or suggest the selection section as recited in claim 1. The Examiner asserts that the selection section is disclosed by the shift register in Sasaki.

Sasaki discloses that the control logic CT includes "a shift register circuit for sequentially selecting the predetermined number of signal lines by shifting, for example, ... an output circuit for setting the signal line selected by the shift register at a potential ..." (emphasis added) (see column 5, lines 12-18).

In contrast, claim 1 requires, "a selection section for selecting one of a signal in synchronization with the timing signal generated by the timing control section and the control data signal input to the data input section, based on the control data signal input to the data input section" (emphasis added).

Therefore, Sasaki appears to disclose a shift register that selects signal lines and sets the signal lines selected at a potential correspond to the pixel data signal, which is in contrast to the selection section for selecting a signal as recited in claim 1.

Furthermore, as shown in Figure 4 of Sasaki, all the inputs, (CLK for transmitting the clock signal, DATA for transmitting the pixel data signal and CNT for transmitting the control signals) via the input pad portion 2, are output from the output pad portion 3 to the next driver IC 1 (see column 4, lines 36-42). Therefore, Applicant submits that no selection of signals exists. More significantly, Applicant has found no disclosure in Sasaki that discloses the selection of any signals input to the driver IC 1 via the input pad portion 2 for output at the output pad portion 3.

Additionally, Applicant submits that Sasaki does not disclose the data output section as recited in claim 1. The Examiner asserts that the data output section as recited in claim 1 is disclosed by the second buffer amplifier 8 and the second latch circuit 7 in Sasaki.

Claim 1 recites, "a data output section for outputting one of the signal in synchronization with the timing signal and the control data signal which is selected by the selection section" (emphasis added).

As discussed above, the Examiner asserts that the selection section is disclosed by the shift register in Sasaki. Even assuming, *arguendo*, that the selection section is disclosed by the shift register, Sasaki still fails to teach or suggest any signal that is selected by the shift register and then outputted by any of the second buffer amplifier 8 and the second latch circuit 7. As previously discussed, there are no logical signal

flow connections permitting signals to flow from control logic CT (which includes the shift register) to output pad portion 3.

Therefore, Sasaki also fails to disclose the data output section as recited in claim 1.

Accordingly, Sasaki fails to teach or suggest claim 1 for at least the above-discussed arguments. Therefore, the rejection of claim 1 under 35 U.S.C. § 102() is improper and should be withdrawn.

Since claims 2-4 are dependent from claim 1, the rejection on these claims should be withdrawn for at least the above-discussed reasons.

Claim 5

Regarding claim 5, Applicant submits that claim 5 is not anticipated by Sasaki for the reasons presented above with respect to claim 1.

Additionally, Applicant submits that Sasaki fails to teach or suggest, "a timing signal for controlling an operation timing of the plurality of column electrode driving circuits and the plurality of row electrode driving circuits is generated in the first column electrode driving circuit...," as recited in claim 5 (emphasis added).

In the rejection of claim 5, the Examiner asserts that the timing signal generated is disclosed by the logic control CT in Sasaki (see page 7 of the Office Action). However, in the "Response to Amendment", the Examiner asserts that the timing signal generated is disclosed by a driving circuit for driving each of the scanning lines ... and driving the signal lines ...; wherein the driving circuit includes a signal line driver ... and the signal line driver includes a plurality of driver ICs ... (see page 14 of Office Action). The Examiner's rejection appears inconsistent and is unclear.

Additionally, the Examiner merely states: "[l]ooking at fig.2, all the IC are connected in a cascading manner where the timing signal controlling the first IC controlling also the last IC." However, this appears to be based on the Examiner's improper interpretation of Figure 2 in Sasaki, and not on the teachings as disclosed by Sasaki.

In particular, Applicant submits that Sasaki discloses an interface unit 25 for entering a power voltage, a pixel data signal, a clock signal and other control signals, supplied from an external liquid crystal controller, a scanning line driver 24 for receiving the power voltage and the control signals from the interface unit 25 ... and includes a pair of signal line 23 for receiving the power voltage, the pixel data signal, the clock signal and the control signals entered by the interface unit 25 to perform at the power voltage ..." (See column 4, line 3-18).

Therefore, the interface unit 25 supplies the scanning line driver 24 and the signal line driver 23 with pixel data signal, clock signal, and other control signal, which does not teach or suggest claim 5.

Furthermore, as previously discussed in more detail, there is no logical signal flow connection permitting signals to flow from control logic CT (which Includes the shift register) to output pad portion 3. Therefore, it appears impossible for the control logic CT to generate a timing control signal for controlling any subsequent driver IC 1.

Therefore, for at least the above-discussed reasons, the rejection of claim 5 should be withdrawn.

Claim 6

Applicant respectfully submits that the rejection of claim 6 also is improper for the same reasons discussed above.

Furthermore, Sasaki also fails to teach or suggest "a timing signal ... output from the first column electrode driving circuit ... is supplied to the first row electrode driving circuit sequentially through a first line portion provided on the tape carrier package ... a second line portion provided on the printed circuit board ... a third line portion provided on the tape courier package ... and a fourth line portion provided on the display ..." as recited in claim 6 (emphasis added).

The Examiner cited column 5, lines 18-29 of Sasaki. However, Applicant cannot see how that cited portion of Sasaki teaches the aforementioned recitation of claim 6. Sasaki merely discloses that the waveforms of the pixel data signal and the control signals are shaped by the latch circuits 5 and 7, and that of the cloak signals are shaped by the latch circuits 5 and 7, and that of the clock signal is shaped by the duty cycle regulator 6.

Applicant submits that Figs. 4 and 13 of Sasaki do not show this feature. Rather, Fig. 4 merely shows the clock line CLK being input from one row/column electrode driving circuit to the next row/column electrode driving circuit. Please let us know if you there are additional features of claim 6 not taught by Sasaki

Therefore, Sasaki fails to teach or suggest claim 6 for at least the above-discussed reasons

Claims 7 and 8

Applicant respectfully submits that the rejections of claims 7 and 8 also are improper for the same reasons discussed above.

Regarding claim 7, Applicant submits that Sasaki does not teach or suggest a timing signal for controlling the plurality of row electrode driving circuits that is

supplied to a row electrode driving circuit sequentially through a second line portion provided on the printed circuit board, a third line portion provided on one of the plurality of column electrode driving circuits, and a fourth line portion provided on the display panel. The Examiner asserts that this feature of claim 7 is disclosed in Figs. 4 and 13 of Sasaki. Applicant submits that Figs. 4 and 13 of Sasaki only show the row or column drivers, and do not disclose the plurality of line portions extending from a column electrode driving circuit to a row electrode driving circuit of claim 7.

Therefore, because Sasaki does not teach each and every feature of independent claims 1, 5, 6, 7 and 8, Sasaki does not anticipate claims 1-8. Thus, the rejection of claims 1-8 under 35 U.S.C. § 102(b) is improper and should be withdrawn.

If the Examiner believes that any of the outstanding issues could be resolved by a telephone interview, the Examiner is kindly invited to call the undersigned at the listed telephone number.

Applicant believes that no additional fees are due for the subject application. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,

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